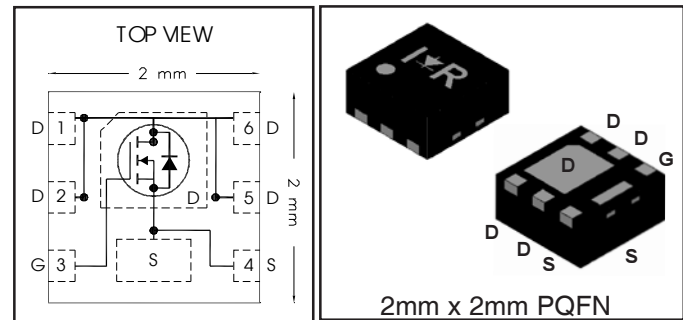


HEXFET® Power MOSFET

$V_{DS}$	<b>30</b>	<b>V</b>
$V_{GS\ max}$	<b>±20</b>	<b>V</b>
$R_{DS(on)\ max}$ (@ $V_{GS} = 10V$ )	<b>16.0</b>	<b>mΩ</b>
$Q_g$ (typical) (@ $V_{GS} = 4.5V$ )	<b>4.2</b>	<b>nC</b>
$I_D$ (@ $T_{c(Bottom)} = 25°C$ )	<b>8.5</b> Ⓢ	<b>A</b>



## Applications

- Control MOSFET for Buck Converters
- System/Load Switch

## Features and Benefits

### Features

Low $R_{DS(on)}$ ( $\leq 16.0m\Omega$ )
Low Thermal Resistance to PCB ( $\leq 13°C/W$ )
Low Profile ( $\leq 1.0\ mm$ )
Compatible with Existing Surface Mount Techniques
RoHS Compliant Containing no Lead, no Bromide and no Halogen
MSL1, Industrial Qualification

results in

### Resulting Benefits

Lower Conduction Losses
Enable better thermal dissipation
Increased Power Density
Easier Manufacturing
Environmentally Friendlier
Increased Reliability

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRFHS8342TRPbF	PQFN 2mm x 2mm	Tape and Reel	4000	
IRFHS8342TR2PbF	PQFN 2mm x 2mm	Tape and Reel	400	EOL notice # 259

## Absolute Maximum Ratings

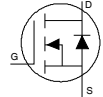
	Parameter	Max.	Units
$V_{DS}$	Drain-to-Source Voltage	30	V
$V_{GS}$	Gate-to-Source Voltage	±20	
$I_D @ T_A = 25°C$	Continuous Drain Current, $V_{GS} @ 10V$	8.8Ⓢ	A
$I_D @ T_A = 70°C$	Continuous Drain Current, $V_{GS} @ 10V$	7.1	
$I_D @ T_{C(Bottom)} = 25°C$	Continuous Drain Current, $V_{GS} @ 10V$	19Ⓢ	
$I_D @ T_{C(Bottom)} = 70°C$	Continuous Drain Current, $V_{GS} @ 10V$	15Ⓢ	
$I_D @ T_{C(Bottom)} = 25°C$	Continuous Drain Current, $V_{GS} @ 10V$ (Package Limited)	8.5Ⓢ	
$I_{DM}$	Pulsed Drain Current ①	76	
$P_D @ T_A = 25°C$	Power Dissipation ④	2.1	W
$P_D @ T_A = 70°C$	Power Dissipation ④	1.3	
	Linear Derating Factor ④	0.02	W/°C
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to +150	°C

Notes ① through ⑤ are on page 2

**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	30	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	22	—	mV/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	13	16	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 8.5A ③②
		—	20	25		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 6.8A ③
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.35	1.8	2.35	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 25μA
ΔV <sub>GS(th)</sub>	Gate Threshold Voltage Coefficient	—	-5.8	—	mV/°C	
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	1.0	μA	V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V
		—	—	150		V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V
g <sub>fs</sub>	Forward Transconductance	18	—	—	S	V <sub>DS</sub> = 10V, I <sub>D</sub> = 8.5A②
Q <sub>g</sub>	Total Gate Charge	—	4.2	—	nC	V <sub>GS</sub> = 4.5V, V <sub>DS</sub> = 15V, I <sub>D</sub> = 8.5A②
Q <sub>gs</sub>	Gate-to-Source Charge	—	1.5	—	nC	V <sub>DS</sub> = 15V
Q <sub>gd</sub>	Gate-to-Drain Charge	—	1.3	—		V <sub>GS</sub> = 10V I <sub>D</sub> = 8.5A② (See Fig. 6 & 16)
Q <sub>oss</sub>	Output Charge	—	3.0	—	nC	V <sub>DS</sub> = 16V, V <sub>GS</sub> = 0V
R <sub>G</sub>	Gate Resistance	—	1.9	—	Ω	
t <sub>d(on)</sub>	Turn-On Delay Time	—	5.9	—	ns	V <sub>DD</sub> = 15V, V <sub>GS</sub> = 4.5V③
t <sub>r</sub>	Rise Time	—	15	—		I <sub>D</sub> = 8.5A②
t <sub>d(off)</sub>	Turn-Off Delay Time	—	5.2	—		R <sub>G</sub> = 1.8Ω
t <sub>f</sub>	Fall Time	—	5.0	—		See Fig.17
C <sub>iss</sub>	Input Capacitance	—	600	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	100	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	46	—		f = 1.0MHz

**Diode Characteristics**

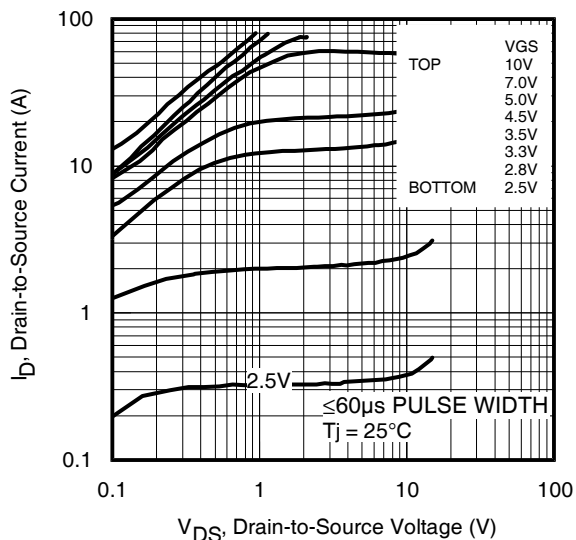
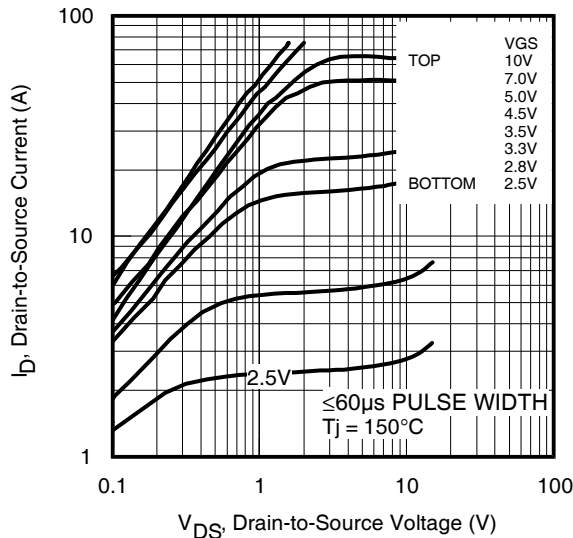
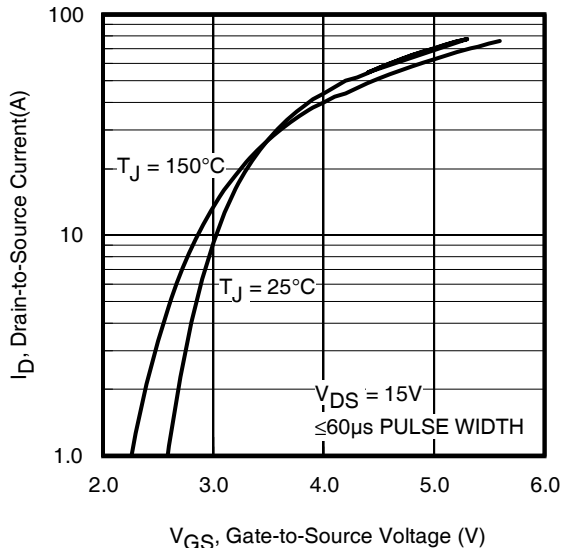
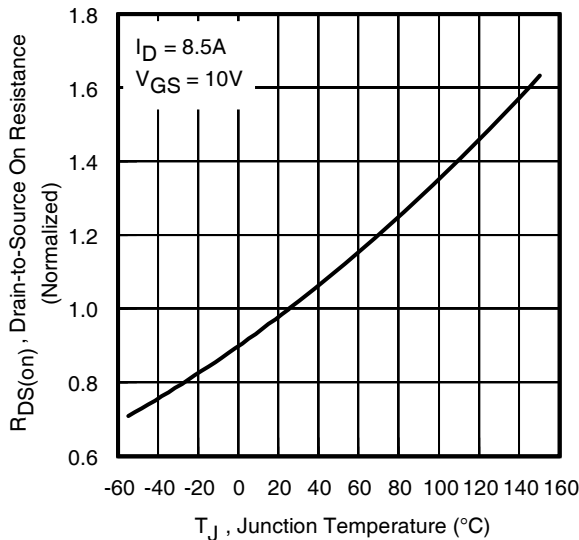
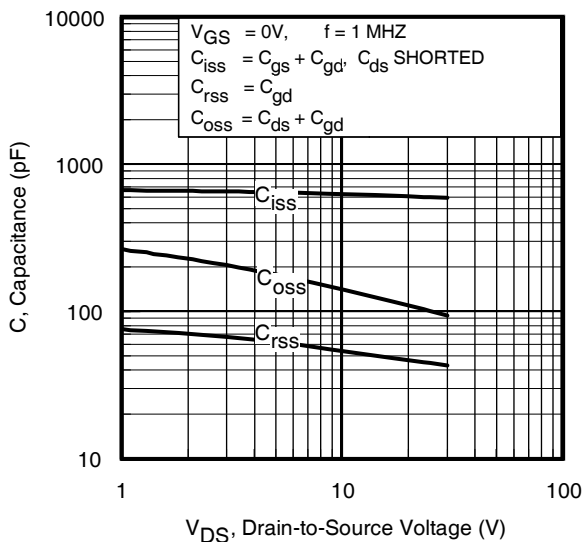
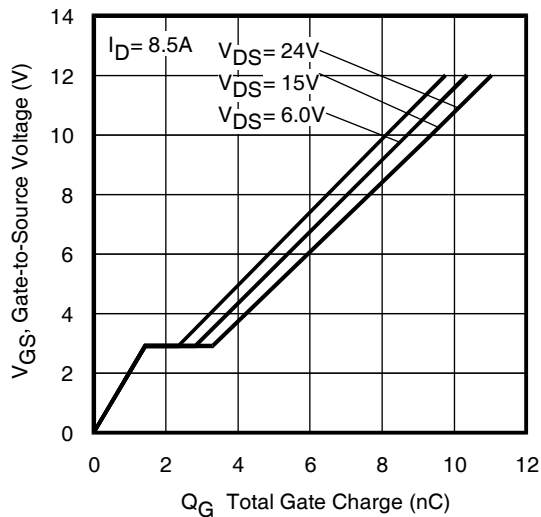
	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	8.5②	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	76		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.0	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 8.5A②, V <sub>GS</sub> = 0V ③
t <sub>rr</sub>	Reverse Recovery Time	—	11	17	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 8.5A②, V <sub>DD</sub> = 15V
Q <sub>rr</sub>	Reverse Recovery Charge	—	13	20	nC	di/dt = 330A/μs ③
t <sub>on</sub>	Forward Turn-On Time	Time is dominated by parasitic Inductance				

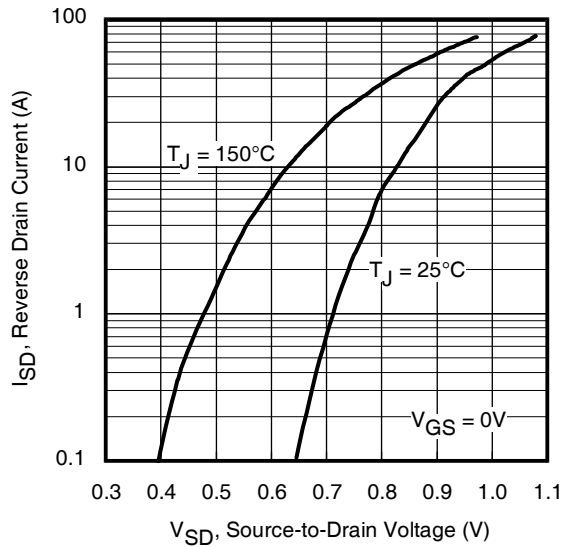
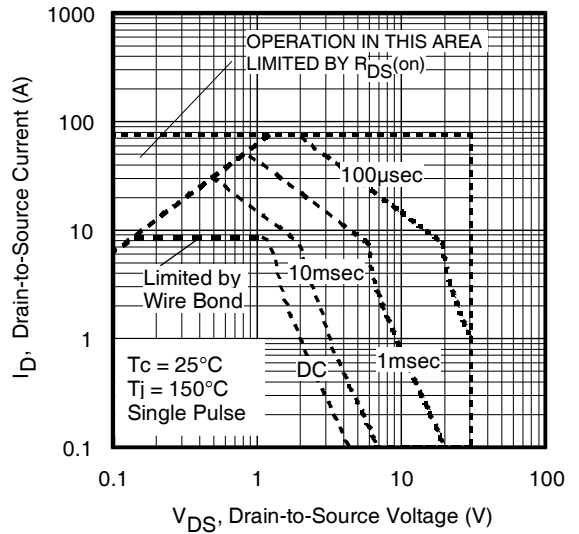
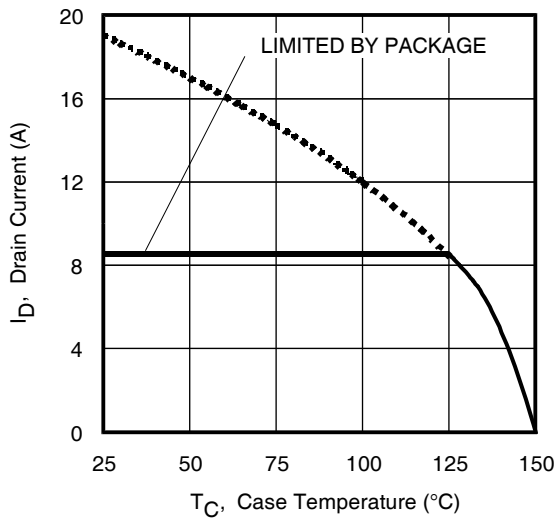
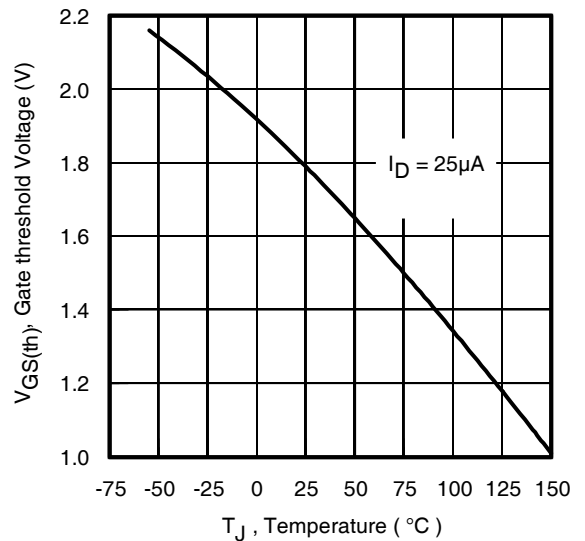
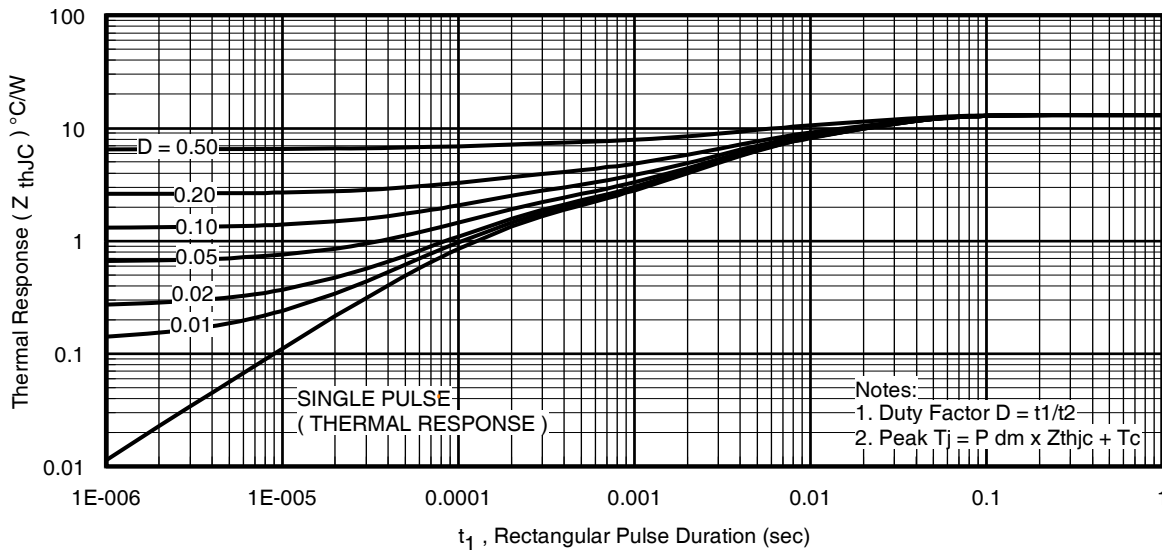
**Thermal Resistance**

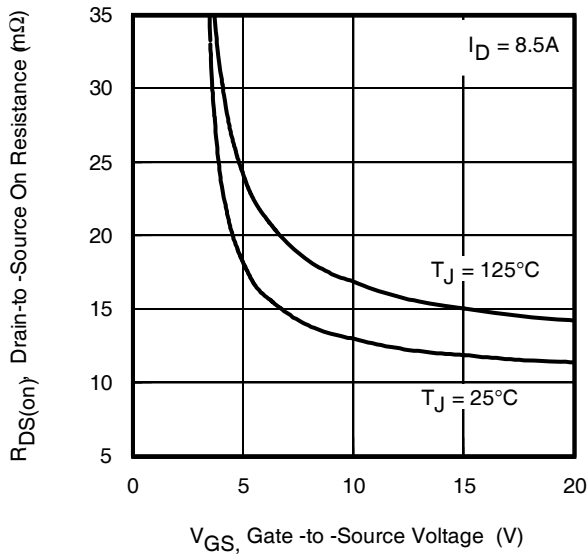
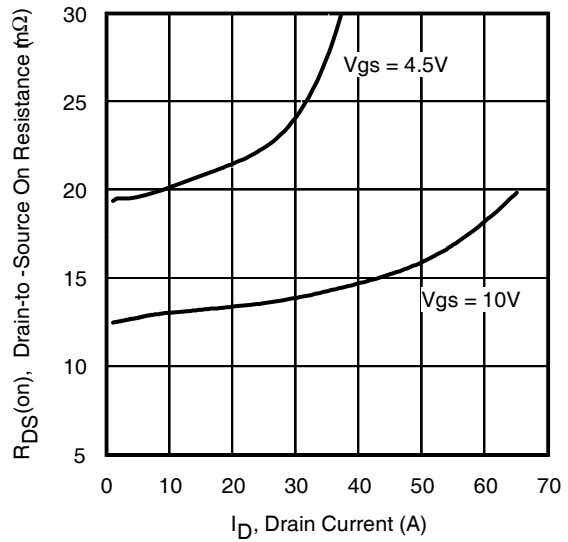
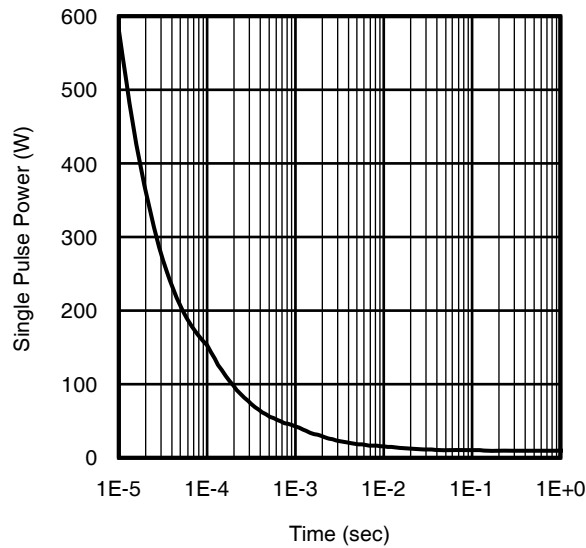
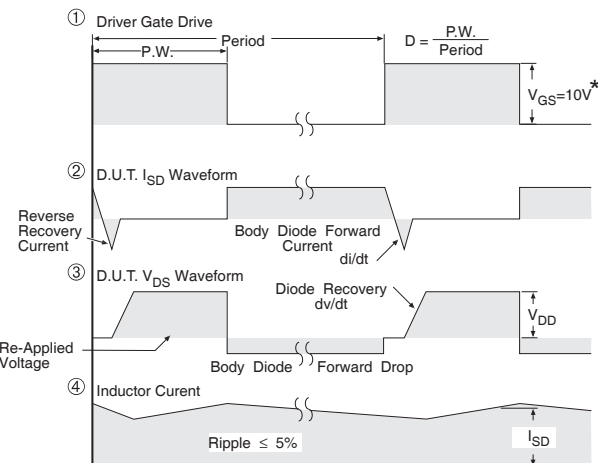
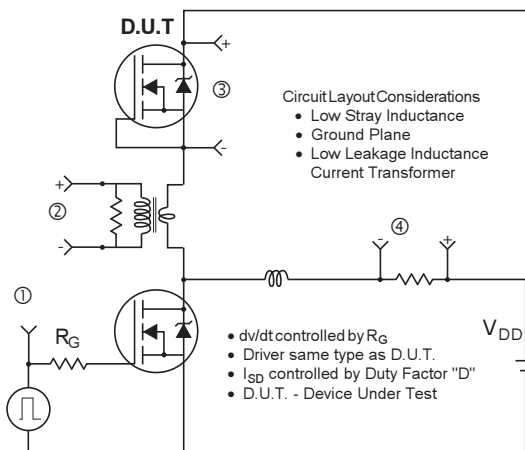
	Parameter	Typ.	Max.	Units
R <sub>θJC</sub> (Bottom)	Junction-to-Case ⑤	—	13	°C/W
R <sub>θJC</sub> (Top)	Junction-to-Case ⑤	—	90	
R <sub>θJA</sub>	Junction-to-Ambient ④	—	60	
R <sub>θJA</sub>	Junction-to-Ambient (<10s) ④	—	42	

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Current limited by package.
- ③ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ④ When mounted on 1 inch square copper board
- ⑤ R<sub>θ</sub> is measured at T<sub>J</sub> of approximately 90°C.


**Fig 1. Typical Output Characteristics**

**Fig 2. Typical Output Characteristics**

**Fig 3. Typical Transfer Characteristics**

**Fig 4. Normalized On-Resistance vs. Temperature**

**Fig 5. Typical Capacitance vs. Drain-to-Source Voltage**

**Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage**


**Fig 7.** Typical Source-Drain Diode Forward Voltage

**Fig 8.** Maximum Safe Operating Area

**Fig 9.** Maximum Drain Current vs. Case (Bottom) Temperature

**Fig 10.** Threshold Voltage vs. Temperature

**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case (Bottom)


**Fig 12. On-Resistance vs. Gate Voltage**

**Fig 13. Typical On-Resistance vs. Drain Current**

**Fig 14. Typical Power vs. Time**


\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 15. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET<sup>®</sup> Power MOSFETs**

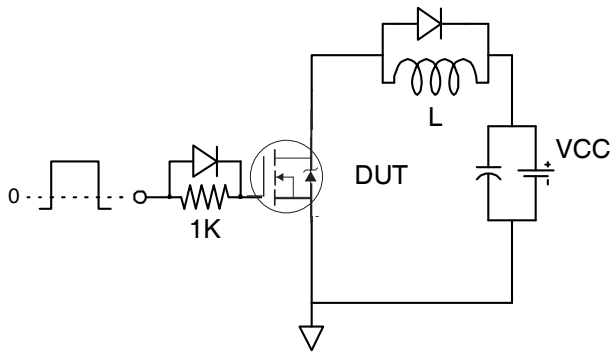


Fig 16a. Gate Charge Test Circuit

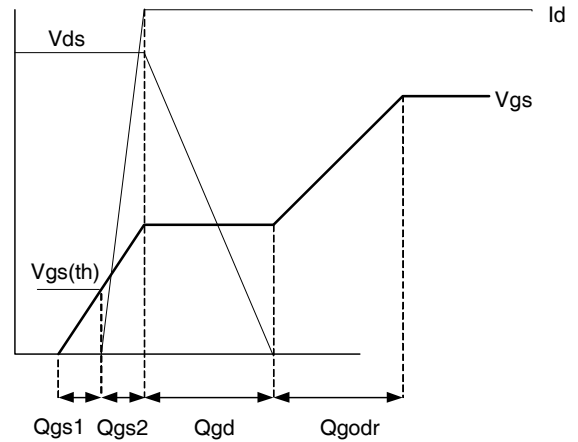


Fig 16b. Gate Charge Waveform

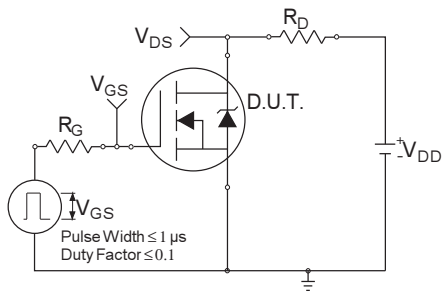


Fig 17a. Switching Time Test Circuit

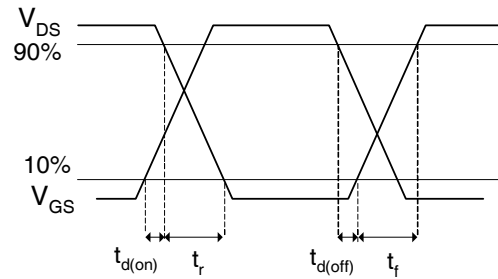
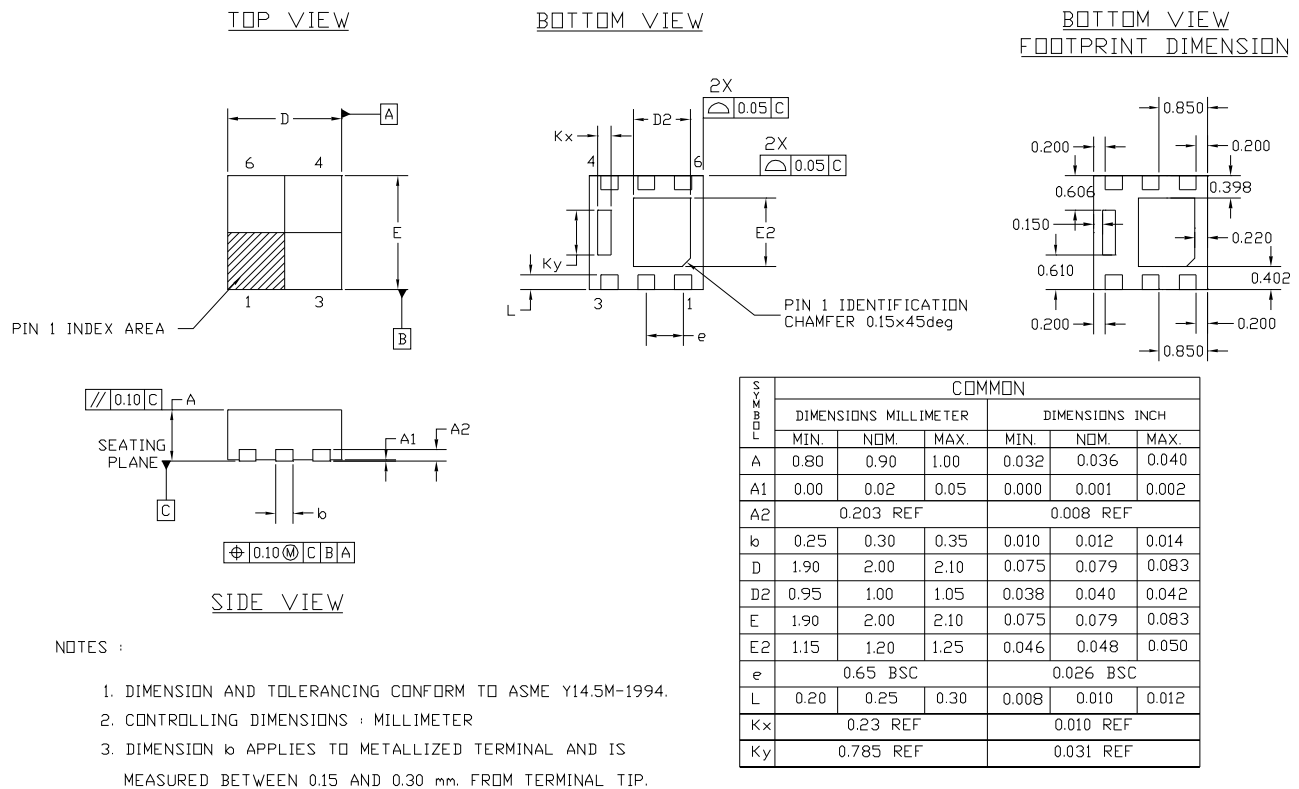


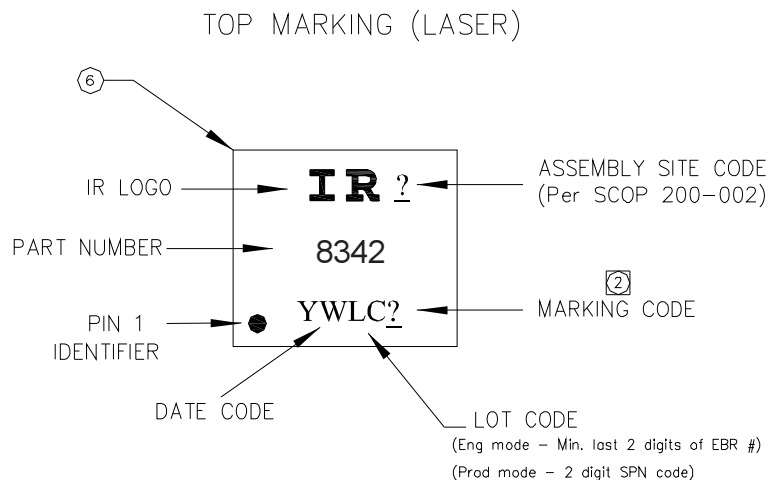
Fig 17b. Switching Time Waveforms

## PQFN 2x2 Outline Package Details



For footprint and stencil design recommendations, please refer to application note AN-1154 at <http://www.irf.com/technical-info/appnotes/an-1154.pdf>

## PQFN 2x2 Outline Part Marking



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

# PQFN 2x2 Outline Tape and Reel

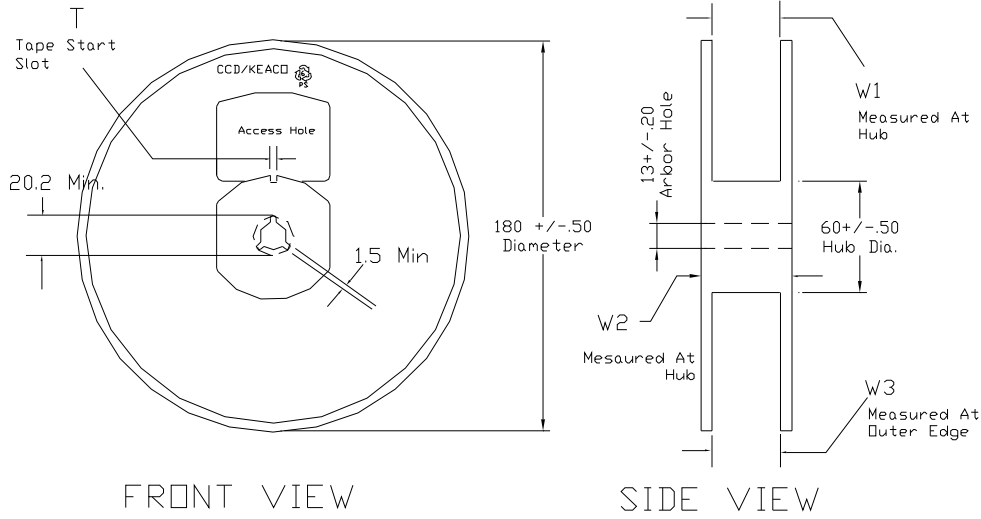
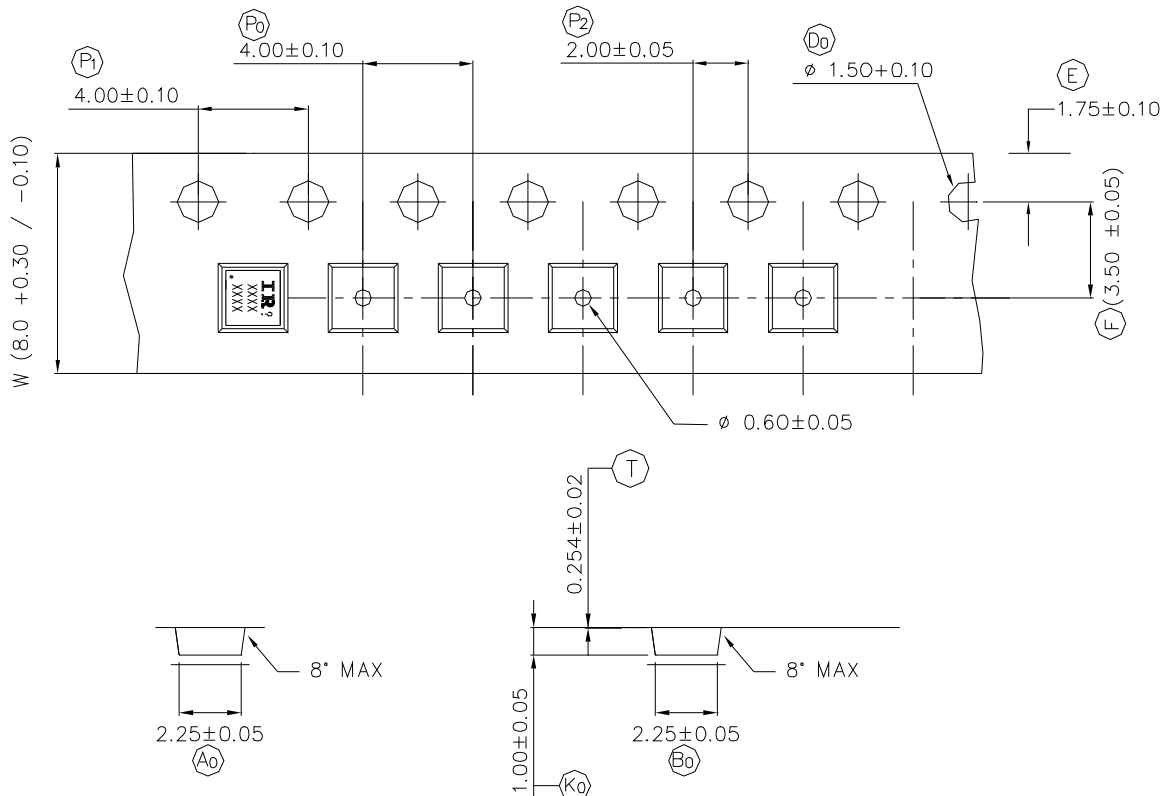


TABLE 1: REEL DETAILS

TAPE WIDTH	T	W1	W2	W3	PART NO
8 MM	3 ± 0.50	8.4 <sup>+1.5</sup> <sub>-0.0</sub>	14.4 Max	7.90 Min 10.9 Max	91586-1
12 MM	5 ± 0.50	12.4 <sup>+2.0</sup> <sub>-0.0</sub>	18.4 Max	11.9 Min 15.4 Max	91586-2

Note: Surface resistivity is  $\geq 1 \times 10^5$  but  $< 1 \times 10^{12}$  ohm/sq.



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>



**Qualification information<sup>†</sup>**

Qualification level	Industrial <sup>†</sup> (per JEDEC JESD47F <sup>††</sup> guidelines)	
Moisture Sensitivity Level	PQFN 2mm x 2mm	MSL1 (per JEDEC J-STD-020D <sup>††</sup> )
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier's web site  
<http://www.irf.com/product-info/reliability>

†† Applicable version of JEDEC standard at the time of product release.

**Revision History**

Date	Comments
9/9/2013	<ul style="list-style-type: none"> <li>• Updated data sheet with new IR corporate template.</li> <li>• Updated Trr/Qrr test condition from "V<sub>DD</sub> = 13V" to "V<sub>DD</sub> = 15V" on page 2</li> </ul>
12/17/2013	<ul style="list-style-type: none"> <li>• Updated ordering information to reflect the End-Of-life (EOL) of the mini-reel option (EOL notice #259)</li> <li>• Updated Qual level from "Consumer" to "Industrial" on page 1, 9</li> </ul>